CLAIMS

1. (Canceled) A switch comprising:

first means responsive to a first set of complementary signals for providing complementary output signals;

second means responsive to the second set of complementary signals for providing complementary output signals; and

third means for selectively activating the first means or the second means in response to a control signal.

2. (Canceled) The invention of Claim 1 wherein said first set of complementary output signals is provided by a master latch.

3. (Canceled) The invention of Claim 2 wherein said second set of complementary signals is provided by a slave latch.

4. (Canceled) The invention of Claim 1 wherein the first means includes a first differential pair of transistors.

5. (Canceled) The invention of Claim 4 wherein the first differential pair of transistors includes first and second transistors Q1 and Q2, respectively.

6. (Canceled) The invention of Claim 5 wherein the first and second transistors are NPN transistors.

7. (Canceled) The invention of Claim 6 wherein the first and second transistors are connected in a common emitter configuration.

8. (Canceled) The invention of Claim 5 wherein the first and second transistors are PNP transistors.

9. (Canceled) The invention of Claim 5 wherein the first and second transistors are field effect transistors.

10. (Canceled) The invention of Claim 5 wherein the first intermediate signal is provided as an input to the first transistor and the second intermediate signal is provided as an input to the second transistor

11. (Canceled) The invention of Claim 5 wherein the second means includes a second differential pair of transistors.

12. (Canceled) The invention of Claim 11 wherein the second differential pair of transistors includes third and fourth transistors Q3 and Q4, respectively.

13. (Canceled) The invention of Claim 12 wherein the third and fourth transistors are NPN transistors.

14. (Canceled) The invention of Claim 13 wherein the third and fourth transistors are connected in a common emitter configuration.

15. (Canceled) The invention of Claim 12 wherein the third and fourth transistors are PNP transistors.

16. (Canceled) The invention of Claim 12 wherein the third and fourth transistors are field effect transistors.

17. (Canceled) The invention of Claim 12 wherein the third intermediate signal is provided as an input to the third transistor and the fourth intermediate signal is provided as an input to the fourth transistor.

18. (Canceled) The invention of Claim 11 wherein the third means includes a third differential pair of transistors.

19. (Canceled) The invention of Claim 18 wherein the third means includes fifth and sixth transistors Q5 and Q6 respectively.

20. (Canceled) The invention of Claim 19 wherein the fifth and sixth transistors are NPN transistors.

21. (Canceled) The invention of Claim 20 wherein the fifth and sixth transistors are connected in a common emitter configuration.

22. (Canceled) The invention of Claim 19 wherein the fifth and sixth transistors are PNP transistors.

23. (Canceled) The invention of Claim 19 wherein the fifth and sixth transistors are field effect transistors.

24. (Canceled) The invention of Claim 19 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals.

25. (Canceled) The invention of Claim 24 wherein the first and sixth transistors have a terminal connected to a source and a terminal connected to one of the first and the second differential pair.

26. (Canceled) The invention of Claim 25 wherein the source is a current source.

27. (Canceled) The invention of Claim 26 wherein the source is a cascode current source.

28. (Canceled) A switch comprising:

first means for providing a first set of first and second complementary intermediate signals;

second means for providing a second set of third and fourth complementary intermediate signals;

third means responsive to the first set of signals for providing complementary output signals;

fourth means responsive to the second set of signals for providing complementary output signals; and

fifth means for selectively activating the third means or the fourth means in response to a control signal.

29. (Canceled) The invention of Claim 28 wherein the first means is a master latch.

30. (Canceled) The invention of Claim 29 wherein the second means is a slave latch.

31. (Canceled) The invention of Claim 30 wherein the slave latch has inputs provided by the master latch.

32. (Canceled) The invention of Claim 28 wherein the third means includes a first differential pair of transistors.

33. (Canceled) The invention of Claim 32 wherein the first differential pair of transistors includes first and second transistors Q1 and Q2, respectively.

34. (Canceled) The invention of Claim 33 wherein the first and second transistors are NPN transistors.

35. (Canceled) The invention of Claim 34 wherein the first and second transistors are connected in a common emitter configuration.

36. (Canceled) The invention of Claim 33 wherein the first and second transistors are PNP transistors.

37. (Canceled) The invention of Claim 33 wherein the first and second transistors are field effect transistors.

38. (Canceled) The invention of Claim 33 wherein the first intermediate signal is provided as an input to the first transistor and the second intermediate signal is provided as an input to the second transistor.

39. (Canceled) The invention of Claim 33 wherein the fourth means includes a second differential pair of transistors.

40. (Canceled) The invention of Claim 39 wherein the second differential pair of transistors includes third and fourth transistors Q3 and Q4, respectively.

41. (Canceled) The invention of Claim 40 wherein the third and fourth transistors are NPN transistors.

42. (Canceled) The invention of Claim 41 wherein the third and fourth transistors are connected in a common emitter configuration.

43. (Canceled) The invention of Claim 40 wherein the third and fourth transistors are PNP transistors.

44. (Canceled) The invention of Claim 40 wherein the third and fourth transistors are field effect transistors.

45. (Canceled) The invention of Claim 40 wherein the third intermediate signal is provided as an input to the third transistor and the fourth intermediate signal is provided as an input to the fourth transistor.

46. (Canceled) The invention of Claim 39 wherein the fifth means includes a third differential pair of transistors.

47. (Canceled) The invention of Claim 46 wherein the fifth means includes fifth and sixth transistors Q5 and Q6 respectively.

48. (Canceled) The invention of Claim 47 wherein the fifth and sixth transistors are NPN transistors.

49. (Canceled) The invention of Claim 48 wherein the fifth and sixth transistors are connected in a common emitter configuration.

50. (Canceled) The invention of Claim 47 wherein the fifth and sixth transistors are PNP transistors.

51. (Canceled) The invention of Claim 47 wherein the fifth and sixth transistors are field effect transistors.

52. (Canceled) The invention of Claim 47 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals.

53. (Canceled) The invention of Claim 52 wherein the first and sixth transistors have a terminal connected to a source and a terminal connected to one of the first and the second differential pair.

54. (Canceled) The invention of Claim 53 wherein the source is a current source.

55. (Canceled) The invention of Claim 54 wherein the source is a cascode current source.

56. (Original) A delta-sigma modulator comprising:

a loop filter;

a comparator coupled to the loop filter; and

a switch, switch comprising:

first means for providing a first set of first and second complementary intermediate signals;

second means for providing a second set of third and fourth complementary intermediate signals;

third means responsive to the first set of signals for providing complementary output signals;

fourth means responsive to the second set of signals for providing complementary output signals; and

fifth means for selectively activating the third means or the fourth means in response to a control signal.

57. (Original) The invention of Claim 56 wherein the first means is a master latch.

58. (Original) The invention of Claim 57 wherein the second means is a slave latch.

59. (Original) The invention of Claim 58 wherein the slave latch has inputs provided by the master latch.

60. (Original) The invention of Claim 56 wherein the third means includes a first differential pair of transistors.

61. (Original) The invention of Claim 60 wherein the first differential pair of transistors includes first and second transistors Q1 and Q2, respectively.

62. (Presently Amended) The invention of Claim 61 wherein the first and second transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

63. (Original) The invention of Claim 62 wherein the first and second transistors are connected in a common emitter configuration.

64. (Presently Amended) The invention of Claim 61 wherein the first and second transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

65. (Original) The invention of Claim 61 wherein the first and second transistors are field effect transistors.

66. (Presently Amended) The invention of Claim 61 wherein [[the]] a first intermediate signal is provided as an input to the first transistor and [[the]] a second intermediate signal is provided as an input to the second transistor.

67. (Original) The invention of Claim 61 wherein the fourth means includes a second differential pair of transistors.

68. (Original) The invention of Claim 67 wherein the second differential pair of transistors includes third and fourth transistors Q3 and Q4, respectively.

69. (Presently Amended) The invention of Claim 68 wherein the third and fourth transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

70. (Original) The invention of Claim 69 wherein the third and fourth transistors are connected in a common emitter configuration.

71. (Presently Amended) The invention of Claim 68 wherein the third and fourth transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

72. (Original) The invention of Claim 68 wherein the third and fourth transistors are field effect transistors.

73. (Presently Amended) The invention of Claim 68 wherein [[the]] a third intermediate signal is provided as an input to the third transistor and [[the]] a fourth intermediate signal is provided as an input to the fourth transistor.

74. (Original) The invention of Claim 67 wherein the fifth means includes a third differential pair of transistors.

75. (Original) The invention of Claim 74 wherein the fifth means includes fifth and sixth transistors Q5 and Q6 respectively.

76. (Presently Amended) The invention of Claim 75 wherein the fifth and sixth transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

77. (Original) The invention of Claim 76 wherein the fifth and sixth transistors are connected in a common emitter configuration.

78. (Presently Amended) The invention of Claim 75 wherein the fifth and sixth transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

79. (Original) The invention of Claim 75 wherein the fifth and sixth transistors are field effect transistors.

80. (Original) The invention of Claim 75 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals.

81. (Original) The invention of Claim 80 wherein the first and sixth transistors have a terminal connected to a source and a terminal connected to one of the first and the second differential pair.

82. (Original) The invention of Claim 81 wherein the source is a current source.

83. (Original) The invention of Claim 82 wherein the source is a cascode current source.

84. (Canceled) A method for switching comprising the steps of:

providing a first set of first and second complementary intermediate signals;

providing a second set of third and fourth complementary intermediate signals;

providing a first set of complementary output signals in response to the first set of signals;

providing a second set of complementary output signals in response to the second set of signals; and

selecting the first or the second set of complementary output signals in response to a control signal.